HP Docket No.: 10017427-1

CLAIMS

What is claimed is:

1	1. A resistive cross point array memory device, comprising:
2	a plurality of word lines extending in a first direction;
3	a plurality of bit lines extending in a second direction such that a
4	plurality of cross points is formed at intersections between the word and bit lines;
5	at least one memory element formed in at least one of the cross points, the
6	memory element comprising a first tunnel junction, the first tunnel junction
7	comprising a bottom conductor, a top conductor, and a barrier layer adjacent the
8	bottom conductor; and
9	wherein the bottom conductor comprises a non-uniform upper surface.
1	2. The memory device of claim 1 wherein the bottom conductor further
2	comprises one of the word lines and the top conductor comprises one of the bit lines.
1	3. The memory device of claim 1 wherein the first tunnel junction is an
2	anti-fuse.
1	4. The memory device of claim 3 wherein the memory element further
2	comprises an isolator element in series with the anti-fuse.
3	
1	5. The memory device of claim 4 wherein the isolator element is selected
2	from the group consisting of a second tunnel junction, a magnetic tunnel junction, a
3	diode and a resistor.

1	6. The memory device of claim 3 wherein the average thickness of the
2	barrier layer is between 10 and 30 angstroms.
1	7. The memory device of claim 3 wherein the barrier layer has a dielectric
2	breakdown voltage of between 2 and 3 volts.
1	8. The memory device of claim 3 wherein the at least one memory
2	element further comprises one of the memory elements formed at each cross point.
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1	9. A tunnel junction for use in a memory element, comprising:
2	a bottom conductor comprising an upper surface;
3	a top conductor;
4	a barrier layer disposed between the bottom conductor and the top conductor;
5	and
6	wherein the barrier layer comprises a non-uniform surface.
1	10. The tunnel junction of claim 9 wherein the tunnel junction is an anti-
2	fuse.
1	11. The tunnel junction of claim 10 wherein the average thickness of the
2	barrier layer is between 10 and 30 angstroms.
1	12. The tunnel junction of claim 10 wherein the barrier layer has a
2	dielectric breakdown voltage of between 2 and 3 volts.

1	13. A method of producing a tunnel junction for use in a memory element,
2	comprising:
3	providing a bottom conductor;
4	creating a non-uniform surface on the barrier layer;
5	depositing a barrier layer on the non-uniform upper surface; and
6	depositing a top conductor such that the barrier layer is disposed between the
7	bottom conductor and the top conductor.
1	14. The method of claim 13 wherein the step of creating a non-uniform
2	upper surface is accomplished using an ion etch technique.
1	15. A memory element comprising:
2	an anti-fuse comprising a bottom conductor, a top conductor, and a barrier
3	layer of non-uniform thickness therebetween;
4	an isolator element in series with the first tunnel junction; and
5	wherein the barrier layer has a dielectric breakdown voltage of between 2 and
6	3 volts.
1	16. The memory element of claim 15 wherein the isolator element is
2	selected from the group consisting of a second tunnel junction, a magnetic tunnel
3	junction, a diode and a resistor.